Si5338

I²C-PROGRAMMABLE ANY-RATE, ANY-OUTPUT QUAD CLOCK GENERATOR

Features

- Single low-jitter PLL with MultiSynth technology enables any-rate frequency synthesis on every output
- Low phase jitter
  - Integer mode: <1 ps rms typ
  - Fractional mode: < 50 ps pp
- Zero ppm frequency error
- Flexible input clock buffer
  - External crystal: 8 to 30 MHz
  - CMOS/SSTL/HSTL clock: 5 to 350 MHz
  - Differential clock: 5 to 700 MHz
- Independently configurable outputs support any frequency, format, voltage
  - LVPECL/LVDS: 0.16 to 700 MHz
  - HCSL: 0.16 to 250 Mhz
  - CMOS: 0.16 to 200 MHz
  - SSTL/HSTL: 0.16 to 350 MHz
  - Voltage: 1.5, 1.8, 2.5, or 3.3 V
  - Four unique frequencies per device enable a maximum of four differential or eight single-ended clock outputs
- Frequency increment/decrement enables continuous, glitchless frequency synthesis (Si5338G/H/J)
- Phase adjustment accuracy of ≤20 ps
- Triangle spread spectrum support
- Optional zero delay buffer mode of operation
- Loss of lock and loss of signal alarms
- I²C/SMBus compatible interface
- Easy to use programming software
- Core supply: 1.8, 2.5, 3.3 V
- Small size: 4 x 4 mm, 24-QFN
- Low power: 45 mA core supply
- Wide temperature range: –40 to +85 °C

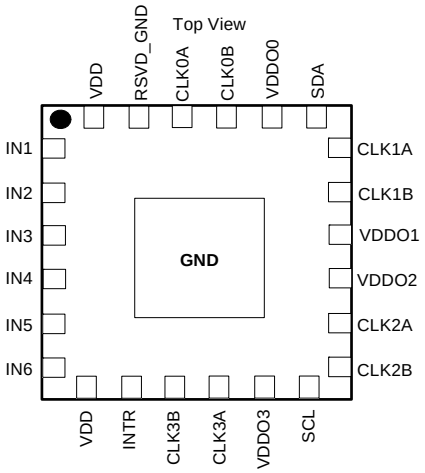
Ordering Information:

See page 28.

Pin Assignments

Si5338

Transparent Top View



Applications

- Gigabit Ethernet
- OC-3/12, SFI-5
- Processor, memory clocking
- PCI Express 2.0
- Broadcast Video
- xDSL
- PON
- T1/E1

Description

The Si5338 is a high-performance, low-jitter clock generator capable of synthesizing any frequency on each of the device's four differential output clocks. The device accepts an external reference clock or crystal and generates four differential clock outputs, each of which is independently programmable to any frequency up to 350 MHz and select frequencies to 700 MHz. Using Silicon Laboratories' patented MultiSynth technology, each output clock is generated with very low jitter and zero ppm frequency error. To provide additional design flexibility, each output clock is independently configurable to support any signal format and supply voltage. The Si5338 provides low jitter frequency synthesis with outstanding frequency flexibility in a space-saving 4 x 4 mm QFN package. The device is programmable via an I²C/SMBus serial interface and supports operation from a 1.8, 2.5, or 3.3 V core supply.

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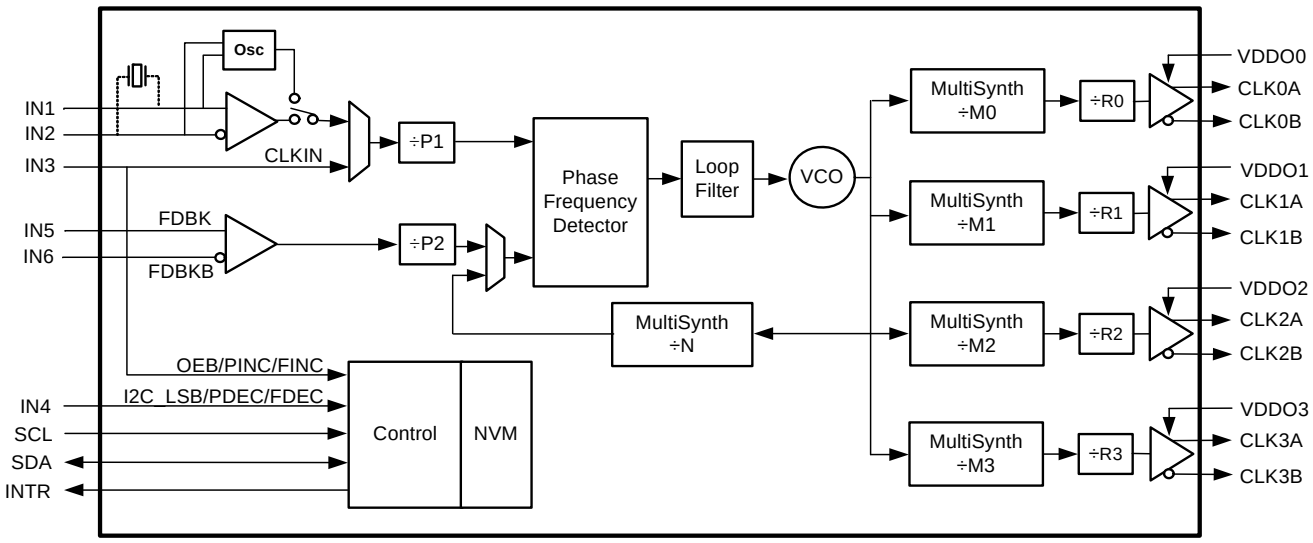
This information applies to a product under development. Its characteristics and specifications are subject to change without notice.

Functional Block Diagram



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1. Electrical Specifications

Table 1. Recommended Operating Conditions

(V_{DD} = 1.8 V –5% to +10%, 2.5 V ±10%, or 3.3 V ±10%, T_A = –40 to 85°C)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit	Notes
Ambient Temperature	T_A		–40	25	85	°C	

Note: All minimum and maximum specifications are guaranteed and apply across the recommended operating conditions. Typical values apply at nominal supply voltages and an operating temperature of 25 °C unless otherwise noted.

Table 2. DC Characteristics

(V_{DD} = 1.8 V –5% to +10%, 2.5 V ±10%, or 3.3 V ±10%, T_A = –40 to 85°C)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Core Supply Voltage	V_{DD}		2.97	3.3	3.63	V
			2.25	2.5	2.75	V
			1.71	1.8	1.98	V
Output Buffer Supply Voltage	V_{DDOn}		1.4	—	3.63	V
Core Supply Current	I_{DD}	100 MHz on all outputs, no load, 25 MHz refclk, see Figure 3	—	—	45	mA
Output Buffer Supply Current	I_{DDOx}	LVPECL, 700 MHz	—	TBD	30	mA
		Low Power LVPECL, 700 MHz	—	TBD	15	mA
		LVDS, 700 MHz	—	TBD	8	mA
		HCSL, 250 MHz 2 pF load capacitance	—	TBD	20	mA
		SSTL, 350 MHz	—	TBD	28	mA
		CMOS, 50 MHz 15 pF load capacitance	—	TBD	28	mA
		CMOS, 200 MHz 2 pF load capacitance	—	TBD	28	mA
		HSTL, 350 MHz	—	TBD	22	mA
Frequency Increment/ Decrement Supply Current	$I_{FINCDEC}$	Freq increment/decrement enabled (1–4 outputs)	—	12	20	mA
VDD POR Threshold Voltage	V_{PORTHR}		—	—	1.55	V
Frequency Synthesis Resolution	f_{RES}	Normal operation	0	0	1	ppb

Notes:
1. See "2.10. R Divider Considerations" on page 19.
2. Maximum frequency may be limited in some configurations

Table 2. DC Characteristics (Continued)
(V_{DD} = 1.8 V –5% to +10%, 2.5 V ±10%, or 3.3 V ±10%, T_A = –40 to 85°C)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Propagation Delay	t_{PROP}	Buffer Mode	—	2.5	—	ns
Output Clock Duty Cycle	t_{ODC}	CLKn < 350 MHz	45	—	55	%
		350 MHz < CLKn < 700 MHz	40	—	60	%
Output-Output Skew	t_{DSKEW}	Outputs at same frequency, signal format	—	—	100	ps
Phase Increment/Decrement Accuracy	P_{STEP}		—	—	20	ps
Phase Increment/Decrement Range	P_{RANGE}		–45	—	+45	ns
Frequency range for phase increment/decrement	f_{PRANGE}		—	—	350[2]	MHz
Phase Increment/Decrement Update Rate[1]	P_{UPDATE}	400 kHz I^2C bus control (Output frequency less than Fvco/8)	—	—	1	kHz
		Pin control	—	—	1500	kHz
Initial Phase Offset	P_{OFFSET}		–45	—	+45	ns
Frequency Increment/ Decrement Step Size	f_{STEP}	R divider not used[1]	0.1	—	10000	kHz
Frequency Increment/ Decrement Range	f_{RANGE}	R divider not used[1]	5	—	350[2]	MHz
Frequency Increment/ Decrement Update Rate	f_{UPDATE}	400 kHz I^2C bus	—	—	1	kHz
		Pin control	—	—	1500	kHz
CLKIN Loss of Signal Detect Time	t_{LOS}		—	2.6	5	µs
CLKIN Loss of Signal Release Time	t_{LOSRLS}		0.01	0.2	1	µs
PLL Loss of Lock Detect Time	t_{LOL}	Clock multiplication ratio off by 1000 ppm	—	5	10	ms
PLL Acquisition Time	t_{ACQ}		—	—	25	ms
PLL Lock Range	f_{LOCK}		5000	—	—	ppm
PLL Loop Bandwidth	f_{BW}		—	1.6	—	MHz

Notes:
1. See "2.10. R Divider Considerations" on page 19.
2. Maximum frequency may be limited in some configurations

Table 2. DC Characteristics (Continued)
(V_{DD} = 1.8 V –5% to +10%, 2.5 V ±10%, or 3.3 V ±10%, T_A = –40 to 85°C)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Reset to Microprocessor Access Ready	m_{RDY}		—	—	2	ms
POR to Output Clock Valid (Pre-programmed Devices)	t_{RDY}		—	—	2	ms
Downspread Spectrum Modulation	SS_{DOWN}	CLKn = 100 MHz	—	–0.5	—	%
Spread Spectrum Modulation Rate	SS_{MOD}	CLKn = 100 MHz	30	—	33	kHz
Spread Spectrum Amplitude Reduction	SS_{RED}	CLKn = 100 MHz	8	—	16	dB

Notes:
1. See "2.10. R Divider Considerations" on page 19.
2. Maximum frequency may be limited in some configurations

Table 3. Input and Output Clock Characteristics
(V_{DD} = 1.8 V –5% to +10%, 2.5 V ±10%, or 3.3 V ±10%, T_A = –40 to 85 °C)

Parameter	Symbol	Test Condition	Min	Typ	Max	Units
Input Clock (AC Coupled Differential Input Clocks on Pins 1, 2, 5, 6)						
Frequency	f_{IN}		5	—	700	MHz
Differential Voltage Swing	V_{PP}		0.5	—	2.4	V_{PP}
Rise/Fall Time	t_R/t_F	20%–80%	—	—	4	ns
Duty Cycle	DC	< 2 ns tr/tf	40	—	60	%
Input Impedance	R_{IN}		10	—	—	kΩ
Input Capacitance	C_{IN}		—	3.5	—	pF
Input Clock (Single-Ended Input Clock on Pins 3 and 4)						
Frequency	f_{IN}	CMOS	5	—	200	MHz
		SSTL/HSTL	5	—	350	MHz
Input Voltage	V_I		–0.1	—	3.63	V
Input Voltage Swing (HSTL Standard)		Input = 350 MHz, Tr/Tf = .6 ns	0.4	—	3.73	V_{PP}
Input Voltage Swing (CMOS Standard)		200 MHz, Tr/Tf = 1.3 ns	0.8	—	3.73	V
Rise/Fall Time	t_R/t_F	20%–80%	—	—	4	ns
Duty Cycle	DC	< 2 ns tr/tf	40	—	60	%
Input Capacitance	C_{IN}		—	2	—	pF

***Note:** R divider must be used for output frequencies < 5 MHz. See "2.10. R Divider Considerations" on page 19.

Table 3. Input and Output Clock Characteristics (Continued)
(V_{DD} = 1.8 V –5% to +10%, 2.5 V ±10%, or 3.3 V ±10%, T_A = –40 to 85 °C)

Parameter	Symbol	Test Condition	Min	Typ	Max	Units
Output Clocks (Differential)						
Frequency*	f_{OUT}	LVPECL, LVDS	0.16	—	350	MHz
			367	—	466	MHz
			550	—	700	MHz
		HCSL	0.16	—	250	MHz
LVPECL Output Option	V_{OC}	common mode	—	V_{DDO} – 1.4 V	—	V
	V_{OD}	diff swing	1.1	1.6	1.92	V_{PP}
LVDS Output Option (2.5/3.3 V)	V_{OC}	common mode	1.125	1.2	1.275	V
	V_{OD}	diff swing	0.50	0.70	0.90	V_{PP}
LVDS Output Option (1.8 V)	V_{OC}	common mode	0.8	0.875	0.95	V
	V_{OD}	diff swing	0.5	0.7	0.9	V_{PP}
HCSL Output Option	V_{OC}	common mode	0.35	0.375	0.400	V
	V_{OD}	diff swing	1.15	1.45	1.7	V_{PP}
Rise/Fall Time	t_R/t_F	20%–80%	—	—	450	ps
Duty Cycle	DC	50% CLKIN duty cycle CKn < 350 MHz	45	—	55	%
		50% CLKIN duty cycle 350 MHz < CLKn < 700 MHz	40	—	60	%

***Note:** R divider must be used for output frequencies < 5 MHz. See "2.10. R Divider Considerations" on page 19.

Table 3. Input and Output Clock Characteristics (Continued)
(V_{DD} = 1.8 V –5% to +10%, 2.5 V ±10%, or 3.3 V ±10%, T_A = –40 to 85 °C)

Parameter	Symbol	Test Condition	Min	Typ	Max	Units
Output Clocks (Single-Ended)						
Frequency*	f_{OUT}	CMOS	0.16	—	200	MHz
		SSTL, HSTL	0.16	—	350	MHz
CMOS 20%-80% Rise/ Fall Time 2 pF load	t_R/t_F	DRVn_SLEW[1:0] = 00	—	0.35	TBD	ns
		DRVn_SLEW[1:0]= 01	—	TBD	TBD	ns
		DRVn_SLEW[1:0] = 10	—	TBD	TBD	ns
		DRVn_SLEW[1:0] = 11	—	TBD	TBD	ns
CMOS Output Resistance			—	50	—	Ω
SSTL Output Resistance			—	50	—	Ω
HSTL Output Resistance			—	50	—	Ω
CMOS Output Voltage	V_{OH}	4 mA load	VDDO–.3			V
	V_{OL}	4 mA load			.3	V
SSTL Output Voltage	V_{OH}	SSTL-3 VDDOx = 2.97 to 3.63 V	.45xVDDO+.41			V
	V_{OL}				.45xVDDO –.41	V
	V_{OH}	SSTL-2 VDDOx = 2.25 to 2.75 V	0.5xVDDO+.41			V
	V_{OL}				0.5xVDDO –.41	V
	V_{OH}	SSTL-18 VDDOx = 1.71 to 1.98 V	0.5xVDDO+.34			V
	V_{OL}				0.5xVDDO –.34	V
HSTL Output Voltage	V_{OH}	VDDO = 1.4 to 1.6 V	0.5xVDDO +.3			V
	V_{OL}				.5xVDDO –.3	V
Input Control Pins (IN3, IN4)						
Input Voltage Low	V_{IL}		–0.1	—	0.3	V
Input Voltage High	V_{IH}		0.9	—	3.63	V
Input Capacitance	C_{IN}		—	—	4	pF
Input Resistance	R_{IN}		20			kΩ
Output Control Pins (INTR)						
Output Voltage Low	V_{OL}	I_{SINK} = 3 mA	0	—	0.4	V
Rise/Fall Time 20–80%	t_R/t_F	C_L < 10 pf, pull up ≤ 1 kΩ	—	—	10	ns

***Note:** R divider must be used for output frequencies < 5 MHz. See "2.10. R Divider Considerations" on page 19.

Table 4. Crystal Specifications for 8 to 11 MHz

Parameter	Symbol	Min	Typ	Max	Unit
Crystal Frequency	f_{XTAL}	8		11	MHz
Load Capacitance (on-chip differential)	c_L	11	12	13	pF
Crystal Output Capacitance	c_O			6	pF
Equivalent Series Resistance	r_{ESR}			300	Ω
Crystal Max Drive Level Spec	d_L	100			µW

Table 5. Crystal Specifications for 11 to 19 MHz

Parameter	Symbol	Min	Typ	Max	Unit
Crystal Frequency	f_{XTAL}	11		19	MHz
Load Capacitance (on-chip differential)	c_L	11	12	13	pF
Crystal Output Capacitance	c_O			5	pF
Equivalent Series Resistance	r_{ESR}			200	Ω
Crystal Max Drive Level Spec	d_L	100			µW

Table 6. Crystal Specifications for 19 to 26 MHz

Parameter	Symbol	Min	Typ	Max	Unit
Crystal Frequency	f_{XTAL}	19		26	MHz
Load Capacitance (on-chip differential)	c_L	11	12	13	pF
Crystal Output Capacitance	c_O			4	pF
Equivalent Series Resistance	r_{ESR}			100	Ω
Crystal Max Drive Level Spec	d_L	100			µW

Table 7. Crystal Specifications for 26 to 30 MHz

Parameter	Symbol	Min	Typ	Max	Unit
Crystal Frequency	f_{XTAL}	26		30	MHz
Load Capacitance (on-chip differential)	c_L	11	12	13	pF
Crystal Output Capacitance	c_O			4	pF
Equivalent Series Resistance	r_{ESR}			75	Ω
Crystal Max Drive Level Spec	d_L	100			µW

Table 8. Jitter Specifications

(V_{DD} = 1.8 V –5% to +10%, 2.5 V ±10%, or 3.3 V ±10%, T_A = –40 to 85 °C)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Random Phase Jitter (12 kHz–20 MHz)	R_J	Output and feedback MultiSynth in Integer mode	—	1	2	ps RMS
Deterministic Phase Jitter	D_J	MultiSynth operated in fractional mode	—	—	20	ps pk-pk
		MultiSynth operated in integer mode	—	—	4	ps pk-pk
Total Jitter (12 kHz–20 MHz)	$T_J = D_J+14xR_J$	MultiSynth operated in fractional mode	—	—	48	ps pk-pk
		MultiSynth operated in integer mode	—	—	32	ps pk-pk
Cycle-Cycle Jitter[1]	t_{CC}	N = 10,000 cycles	—	—	60	ps pk-pk
Period Jitter[1]	t_{PERIOD}	CLKIN = 25 MHz All CLKns at 100 MHz	—	30	50	ps pk-pk
PCI Express 2.0 Random Phase Jitter (1.5 MHz—50 MHz)	R_J	CLKIN = 25 MHz All CLKns at 100 MHz Spread Spectrum not enabled.	—	TBD	2	ps RMS
OC-12 RMS Phase Jitter (12 kHz—5 MHz)	R_{JOC12}	CLKIN = 19.44 MHz All CLKns at 155.52 MHz	—	TBD	2	ps RMS
GbE RMS Phase Jitter (1.875—20 MHz)	R_{JGBe}	CLKIN = 25 MHz All CLKns at 125 MHz	—	TBD	2	ps RMS

Notes:
1. Tested with Agilent 90804 oscilloscope. See “AN357: Optimized Time Domain Clock Jitter Measurements”.
2. All jitter measurements are with LVDS output format.

Table 9. I²C Specifications (SCL,SDA)[2]

Parameter	Symbol	Test Condition	Standard Mode		Fast Mode[3]		Unit
			Min	Max	Min	Max	
LOW level input voltage:	V_{ILI2C}		–0.5	$0.3*V_{DDI2C}$	–0.5	$0.3*V_{DDI2C}$[1]	V
HIGH level input voltage:	V_{IHI2C}		$0.7*V_{DDI2C}$	3.63	$0.7*V_{DDI2C}$[1]	3.63	V

Notes:
1. Only I²C pull up voltages (VDDI2C) of 1.71 to 3.63 V are supported.
2. Refer to NXP’s UM10204 I²C-bus specification and user manual, revision 03, for further details: www.nxp.com/acrobat_download/usermanuals/UM10204_3.pdf.
3. Compliant with Fast Mode+ pending characterization.

Table 9. I²C Specifications (SCL,SDA)[2] (Continued)

Parameter	Symbol	Test Condition	Standard Mode		Fast Mode[3]		Unit
Hysteresis of Schmitt trigger inputs	V_{HYS}		N/A	N/A	0.1	—	V
LOW level output voltage (open drain or open collector) at 3 mA sink current	V_{OLI2C}[1]	V_{DDI2C}[1] = 2.5 / 3.3 V	0	0.4	0	0.4	V
		V_{DDI2C}[1] = 1.8 V	N/A	N/A	0	0.2 x V_{DDI2C}	V
Input current	I_{II2C}		–10	10	–10	10	µA
Capacitance for each I/O pin	C_{II2C}	V_{IN} = –0.1 to V_{DDI2C}	—	4	—	4	pF
I²C Bus timeout	—	Timeout Enabled	25	35	25	35	msec

Notes:
1. Only I²C pull up voltages (VDDI2C) of 1.71 to 3.63 V are supported.
2. Refer to NXP's UM10204 I²C-bus specification and user manual, revision 03, for further details: www.nxp.com/acrobat_download/usermanuals/UM10204_3.pdf.
3. Compliant with Fast Mode+ pending characterization.

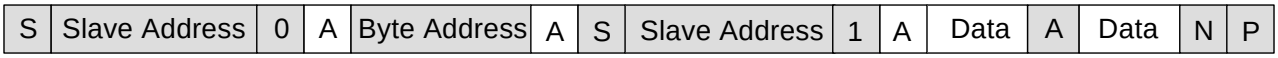


Figure 1. I²C/SMBus-Compatible Read Command

From master to slave

From slave to master

1 – Read
2 – Write
A – Acknowledge (SDA LOW)
N – Not Acknowledge (SDA HIGH).
Required after the last data byte to signal the end of the read comand to the slave.
S – START condition
P – STOP condition

Figure 2. I²C/SMBus-Compatible Write Command

Table 10. Thermal Characteristics

Parameter	Symbol	Test Condition	Value	Unit
Thermal Resistance Junction to Ambient	Theta JA	Still Air	37	°C/W

Table 11. Absolute Maximum Ratings

Parameter	Symbol	Test Condition	Value	Unit
DC Supply Voltage	V_{DD}		–0.5 to 3.8	V
Storage Temperature Range	T_{STG}		–55 to 150	°C
ESD Tolerance		HBM (100 pF, 1.5 kΩ)	2	kV
ESD Tolerance		CDM	550	V
ESD Tolerance		MM	175	V
Latch-up Tolerance			JESD78 Compliant	

Note: Permanent device damage may occur if the Absolute Maximum Ratings are exceeded. Functional operation should be restricted to the conditions as specified in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

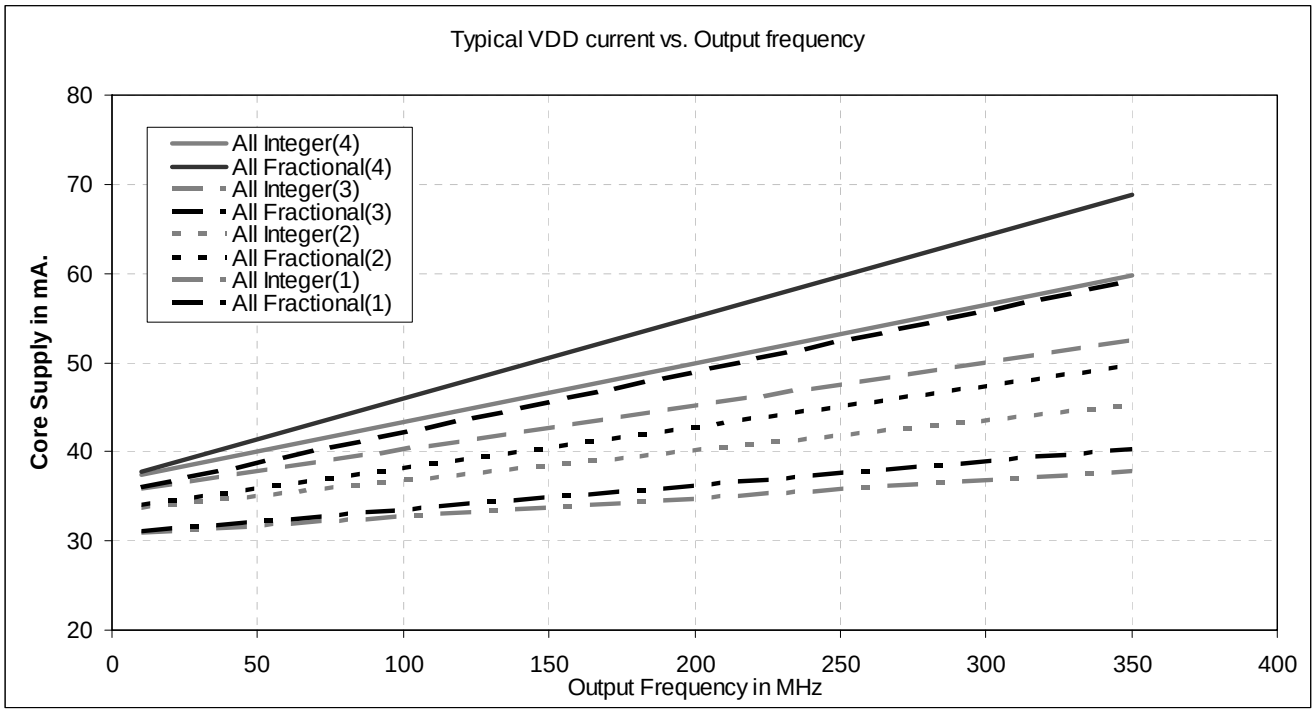


Figure 3. Core Supply Current vs. Output Frequency

2. Functional Description

2.1. Overview

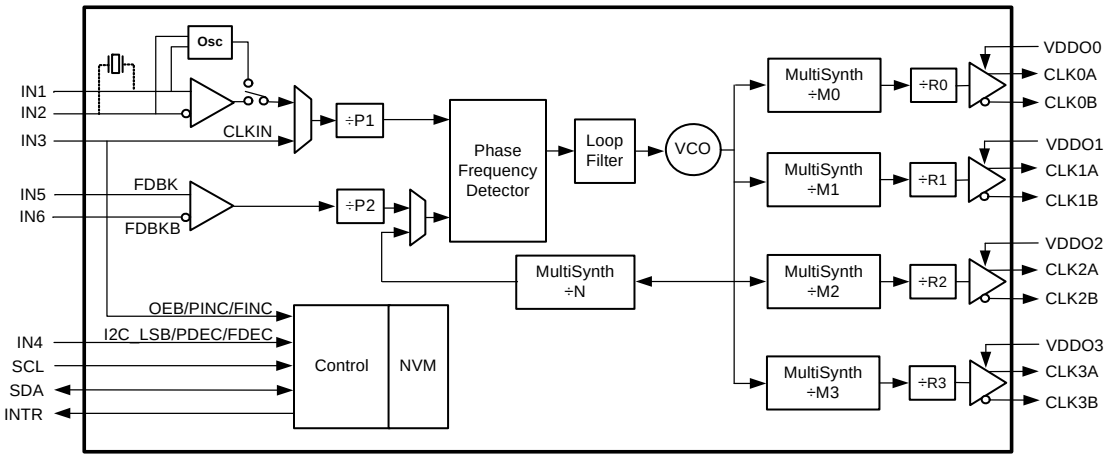


Figure 4. Si5338 Block Diagram

The Si5338 is a high performance, low jitter clock generator capable of synthesizing any frequency ranging from 0.16 to 350 MHz on each of the device's four differential output clocks. The device accepts an external crystal from 8 to 30 MHz or an input clock ranging from 5 to 700 MHz. Each output is independently user-programmable to any frequency up to 350 MHz and select frequencies to 700 MHz. Each differential output clock can optionally be configured to produce two single-ended clocks at the same frequency, so a total of eight clock outputs at four unique frequencies are available.

The Si5338 fractional-N PLL, comprised of a phase detector, charge pump, loop filter, VCO, and dividers, is fully integrated on chip to simplify design. Using Silicon Laboratories' patented MultiSynth technology, each output clock is generated with < 2 ps rms phase jitter and zero ppm frequency error. The device has four MultiSynth output dividers to provide non-integer frequency synthesis on every differential output clock.

The Si5338 output driver is highly flexible. The signal format of each differential output clock can be user-specified to support LVPECL, LVDS, HCSL, CMOS, HSTL, or SSTL. If a single-ended format is selected, two in-phase outputs are generated per differential buffer. In addition, each differential output clock is supplied with an independent supply voltage ranging from 1.4 to 3.63 V such that the device can be used in mixed supply applications without the need for external level translators. When an output clock is configured to be a CMOS format, the slew rate can be user-programmed. This slew rate control can be used to minimize EMI on a per output clock basis.

The ability to invert output clocks is supported regardless of the format.

The Si5338 supports an optional zero delay buffer mode (ZDB) of operation. In this mode, one of the device output clocks is fed back to the FDBK/FDBKB clock input pins to implement the PLL feedback path and nullify the phase difference between the reference input and the output clocks.

The Si5338 has a digitally controlled phase increment/decrement feature that allows the user to adjust the phase of each output clock in relation to the other output clocks. The phase of each differential output clock can be set to an accuracy of 20 ps over a range of ±45 ns. This feature is available over the 0.16 to 350 MHz frequency range. Register control of this feature is available via the microprocessor interface. This feature is also available via pin control in some Si5338 variants as listed in Table 10.

The Si5338 has a digitally-controlled frequency increment/decrement feature that allows the user to dynamically transition from one frequency to another in a programmable number of steps. This feature is available over the 0.16 to 350 MHz frequency range. The frequency transition is continuous and glitchless. This feature is useful in applications that require a continuous, variable clock frequency. It can also be used in frequency margining applications to margin test system clocks during design/verification/test or manufacturing test applications. Register control of this feature is available via the microprocessor interface. This feature is also available via pin control in some Si5338 variants as listed in Table 10.

For noise reduction, the Si5338 supports spread spectrum clocking (SSC). Down spread of –0.5% is available in compliance with PCI Express 2.0 specifications. Spread spectrum is available on all output clocks and can be individually turned on/off for each differential output clock via the I^2C interface. This feature is available when the output clocks are configured for 100 MHz operation.

The device is programmable via an I^2C/SMBus compatible interface. The device has a maskable interrupt output alarm pin which can be monitored for PLL loss of lock, input clock loss of signal, and feedback clock loss of signal conditions. The Si5338 may be operated from a 1.8, 2.5, or 3.3 V core supply. All device specifications are guaranteed across these three core supply voltages. Packaged in a ROHS-6, Pb-free 4 x 4 mm QFN package, the device supports the industrial temperature range of –40 to +85 °C.

After a power-on reset, the Si5338 reads the contents of its non-volatile memory (NVM) and begins operation using these parameters. By default, the Si5338 NVM is blank and the device must be written via the I^2C interface before the PLL acquires lock and generates output clocks. Optionally, the default operating condition can be user-specified and either factory-programmed or field-programmed into the device NVM. This feature is one-time programmable. In this mode, no user intervention is required before the device begins operation at the start-up configuration. A wide range of input clock frequency, output clock frequencies, and output clock signal formats is supported in this mode of operation.

2.2. Si5338 Configuration Software and Programmer's Kit

Silicon Labs offers Si5338 configuration software to simplify frequency planning and device programming. Simply specify the desired input and output frequencies and the software automatically calculates the VCO frequency and PLL divider combination that yields the lowest jitter and lowest power. This software is available for download from www.silabs.com/timing. This software is also available with the device evaluation board, Si5338-EVB and the device programmer, Si5338-PROG-EVB.

The Si5338-EVB is the standard evaluation board for the device and includes an Si5338 device soldered down on the board. The Si5338-PROG-EVB programming kit includes a socketed board and five blank Si5338 devices which can be field-programmed by the user to specify different start-up configurations. Upon a subsequent power-on reset, the device will come up in the field-programmed configuration. Contact your local Silicon Labs sales representative for further details regarding a Si5338 I^2C-programmable clock generator with a factory-programmed default operating configuration.

The Si5338 software and the programming kit may also be used to generate custom Si5334 pin-controlled clock generators. Consult the Si5338-PROG-EVB data sheet or the Si5334 data sheet for further details. The Si5338 is always programmable in-circuit via the I^2C interface.

The remainder of the functional description contains details only needed when the Si5338 configuration software is not used to program the device.

2.3. Crystal/Input Clock

The device can be driven from either a low frequency fundamental mode crystal (8–30 MHz) or an external reference clock (5–700 MHz). The crystal is connected across pins IN1 and IN2.

The PCB traces between the crystal and the device must be kept very short to minimize stray capacitance. To ensure maximum compatibility with crystals from multiple vendors, the internal crystal oscillator provides adaptive crystal drive strength based upon the crystal frequency. This feature provides interoperability with any 8–30 MHz crystals with equivalent series resistance (ESR) values ranging from 30 to 80 Ω.

The crystal load capacitors are placed on-chip to reduce external component count. If a crystal with a load capacitance outside the range specified in Table 3 is supplied to the device, it will result in a slight ppm error in the device clock output frequencies. The Si5338 configuration software calculates the ppm error for each output clock based on the crystal load capacitance and can be used to null this ppm error if so desired. Consult the Si5338 configuration software for more details.

If a reference clock is used, the device accepts a single-ended input reference from a CMOS, HSTL, or SSTL source on IN3 or a differential LVPECL, LVDS, or HCSL source on IN1 and IN2. The input at IN3 is internally AC coupled and will tolerate 3.63 V regardless of the core VDD supply voltage. The signal applied at IN3 should be dc-coupled. If a differential input clock is input a 100 Ω resistor should be located very close to the device and between IN1 and IN2. The differential signal must be AC coupled to IN1 and IN2.

The Si5338 can operate as a clock generator or a zero delay buffer. By default the device is configured for clock generator mode. If zero delay buffer mode is used, one of the device output clocks is routed to the feedback clock input pins. The feedback clock can be single-ended (CMOS, HSTL, or SSTL) or differential (LVPECL, LVDS, or HCSL). The signal format of the

input clock and output clocks must be the same in the zero delay buffer mode of operation.

It is recommended to use CLK3 as the feedback source to minimize the routing length.

For differential feedback, the CLK3A,B pins should be routed to the N5,6 pins, respectively. For single-ended feedback, CLK3A should be dc-connected to IN4.

The input at IN4 is internally AC coupled and will tolerate 3.63 V regardless of the VDD supply voltage. The signal applied at IN4 should be dc-coupled. An input applied to IN5 and IN6 must be ac coupled and a 100 Ω resister should be placed between IN5 and IN6 and located very close to the device pins.

Unused input clocks must be connected to ground. Consult “AN408: Si5338 I/O Termination Guidelines” for clock input and clock output termination guidelines for the Si5338.

2.4. Clock Multiplication Settings

Using Silicon Laboratories' patent-pending MultiSynth technology, the Si5338 can generate up to four unique non-integer related output frequencies on up to eight clock outputs with zero ppm frequency error. Each output is independently user-programmable to any frequency up to 350 MHz and select frequencies to 700 MHz. Note that if one or more output clocks are configured to be >350 MHz, then the maximum frequency of the remaining output clocks may be limited to the range of 275–350 MHz. Consult the Si5338 configuration software for more details.

Independent, non-integer related output frequencies are easily configured by selecting a unique MultiSynth output divider value M for each output clock. The MultiSynth output and feedback dividers are fractional dividers expressed in terms of an integer and a fraction.

The resolution of the fractional part is the ~$1e^{-9}$, which means that, for all intents and purposes, the output frequency can be defined exactly from the input frequency. The input to output frequency transfer equation is as follows:

$$f_{OUT} = \frac{f_{IN} \times N}{Pn \times M \times Rn}$$

where:

f_{OUT} = Output frequency

f_{IN} = Input frequency

Pn = Input divider P1 or P2

Values of 1, 2, 4, 8, 16, and 32 are supported

Rn = Output divider R0, R1, R2, or R3

Values of 1, 2, 4, 8, 16, and 32 are supported

N = MultiSynth feedback divider

M = MultiSynth output divider

Full integer values in the MultiSynth dividers always provide the best jitter performance and lower power. Following a manual change in any divider value, the device must be reset using the SOFT_RESET register to make the change effective. When the Rn divider is not set to 1, the output phase for that channel may initiate to an incorrect value. Additionally, since the frequency increment and decrement function is referenced to the output of the MultiSynth, non-unity Rm divider settings will affect the expected frequency change from an increment and decrement. The phase increment and decrement function is unaffected by the Rn divider setting.

There may be multiple valid combinations of divider values for a particular frequency plan. To simplify device configuration, Silicon Labs provides Si5338 software that determines the valid combinations and selects the optimum PLL divider settings based on jitter performance and power consumption. The Si5338 software can be downloaded from www.silabs.com/timing.

2.5. Breakthrough MultiSynth Technology

Next-generation timing architectures require a wide range of frequencies which are often non-integer related. Traditional clock architectures address this by using multiple single PLL ICs, often at the expense of BOM complexity and power. The Si5334 and Si5338 use patented MultiSynth technology to dramatically simplify timing architectures by integrating the frequency synthesis capability of 4 Phase-Locked Loops (PLLs) in a single device, greatly minimizing size and power requirements versus traditional solutions. Based on a fractional-N PLL, the heart of the architecture is a low phase noise, high frequency VCO. The VCO supplies a high frequency output clock to the MultiSynth block on each of the four independent output paths. Each MultiSynth operates as a high speed fractional divider with Silicon Laboratories' proprietary phase error correction to divide down the VCO clock to the required output frequency with very low jitter.

The first stage of the MultiSynth architecture is a fractional-N divider which switches seamlessly between the two closest integer divider values to produce the exact output clock frequency with 0 ppm error. To eliminate phase error generated by this process, MultiSynth calculates the relative phase difference between the clock produced by the fractional-N divider and the desired output clock and dynamically adjusts the phase to match the ideal clock waveform. This novel approach makes it possible to generate any output clock frequency without sacrificing jitter performance. Based on this architecture, the output of each MultiSynth can produce any frequency from 5 to fvco/8 MHz. Since the maximum VCO frequency is 2.8 MHz, the maximum frequency at the output of the MultiSynth is 350 MHz. To support higher frequency operation, the MultiSynth divider can be bypassed. In bypass mode integer divide ratios of 4 and 6 are supported, which allows for output frequencies of fvco/4 and fvco/6 MHz which translates to 367–466 MHz and 550-700 MHz respectively. Because each MultiSynth uses the same VCO output there can be output frequency limitations due to the frequency plan. If a frequency of 375 MHz is needed, the VCO would need to be at 2.25 GHz and the MultiSynth must be bypassed to achieve an output frequency > 350 MHz. Since the VCO frequency is 2.25 GHz, that means that all the other CLKn outputs can have a maximum frequency of FVCO/8 or 281.25 MHz. The Si5338 Programmer software takes all of this, and more, into consideration in order to allow frequency plans to be quickly and easily synthesized.

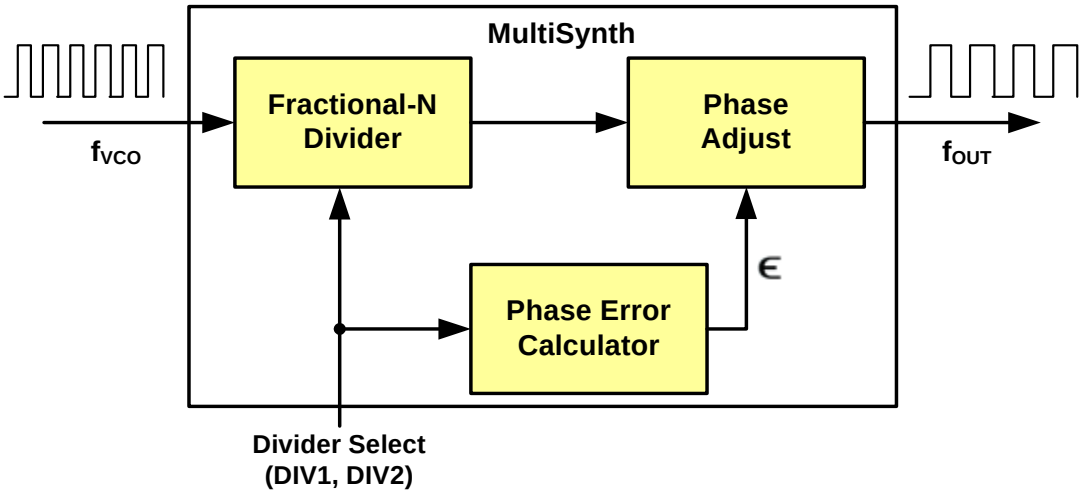


Figure 5. Silicon Labs' MultiSynth Technology

2.6. Output Driver

There are four clock output channels on the Si5338 (CLK0,CLK1,CLK2,CLK3) with two signal outputs per channel. Each channel may be programmed to be a differential driver or a dual single ended driver. If a channel is programmed to be single ended, then the two outputs will default to being in phase however either output can be inverted or turned off. A differential channel output can have both outputs inverted together or turned off. Si5338 output drivers can be configured as single ended CMOS, SSTL, HSTL or differential LVPECL, LVDS, and HCSL formats. The CMOS output driver also has programmable rise/fall time from ~1ns to ~4 ns. A special low power LVPECL driver format is available which does not require the typical low value resistor for DC bias.

The supply voltage requirement for each driver format should also be set using the Si5338 programmer

software. All unused clock output channels must have their respective VDD0x supply voltage connected to pin 7 and 24 VDD. See Table 12 for the available options.

If an output driver is not used the entire channel may be powered down to save the most current. Alternately each output driver may be disabled individually or all drivers may be disabled simultaneously. When an output driver is disabled there is a choice to have the output be a high, low or high Z. For a better understanding of the output driver capabilities of the Si5338 please read AN408. Complete control of the output drivers is simplified by using the Si5338 Programmer software.

2.7. Output Clock Initial Phase Offset

The Si5338 supports programmable phase adjustment between output clocks with an accuracy of at least 20 ps. This feature can be used to compensate for trace length mismatches between different output clocks. Phase offset is independently programmable for every output clock. The phase adjustment range is ±45 ns. The initial phase of each clock output is also configurable with an accuracy of 20 ps. The Si5338 configuration software should be used to calculate the correct phase offset value in conjunction with the VCO clock rate for a given frequency plan. Once the device output clock initial phase offset is programmed, a subsequent soft reset will not change this phase offset. When the Rn divider is not set to 1, the initial phase offset function is not supported.

2.8. Output Clock Phase Increment/Decrement

The Si5338 has a digitally-controlled phase increment/decrement feature that allows the user to adjust the phase of each output clock in relation to the other output clocks. The phase of each output clock can be adjusted with an accuracy of < 20 ps over a range of ±45 ns. The maximum clock output frequency supported in this mode of operation is $f_{VCO}/8$, where f_{VCO} is the frequency of the device's internal Voltage Controlled Oscillator for the configured frequency plan. The phase transition is glitchless. The Si5338 programmer must be used to set the magnitude of the phase step and calculate the register values for the phase increment/decrement feature. This feature is also available via pin control for the Si5338D/Si5338E/Si5338F and will allow the phase to increment or decrement up to a rate of 1 MHz.

When pin control is desired, pins 1 and 2 must be used for the input clock (crystal) so that the IN3 and IN4 pins are available for increment/decrement. Pin control of phase requires a positive pulse that is greater than 100 ns followed by at least 100 ns of low level. Pin control of phase increment or decrement can apply to one or more of the outputs. Each clock output can be programmed to change phase with different step sizes. The NVM can be programmed at the factory to set the magnitude of the phase increment and to which outputs it is applicable. Using pin control, the latency (phase) can be incremented as fast as 100 kHz. The magnitude of the change must be set using the Si5338 programmer.

I^2C control of phase increment and decrement is also possible on all Si5338 devices and necessary on the Si5338A,B,C,G,H,J as these devices do not provide pin-controlled phase adjustment. Using the I2C interface will allow the phase of each output clock to be independently controlled.Table 13 lists the registers that control activation of phase increment and decrement.

Table 12. Output Driver Signal Format Selection

VDD0x Supply Voltage	CMOS	SSTL	HSTL	LVPECL	LVPECL low power	LVDS	HCSL
1.5			X				
1.8	X	X				X	X
2.5	X	X		X	X	X	X
3.3	X	X		X	X	X	X

Registers 52,63,74,85 control the clock outputs CLK0,1,2,3 respectively. Each single write of 01 to the CLKnPHASESTEPCTRL[1:0] will cause the phase to be incremented. Likewise a write of 10 will decrement the phase.

Table 13. Output Clock Phase Control

CLKnPHASESTEPCTRL[1:0] Registers 52,63,74,85[1:0]	Output Phase
00	Disable all phase increment/decrement and reset phase to the initial phase offset value.
01	Enable pin control of phase inc/dec
10	Phase is incremented
11	Phase is decremented

2.9. Output Clock Frequency Increment/Decrement

The Si5338 has a digitally controlled frequency increment/decrement feature that allows the user to transition from one frequency to another either by pin control or I^2C writes. The step size for the frequency increment and decrement is from 0.1 kHz to 10 MHz. Each channel output can be independently set for the size of the frequency step and whether or not the channel responds to pin control of frequency. Pin control of frequency is available on Si5338G/H/J. All Si5338 devices allow I^2C control of frequency increment/decrement. The frequency transition is always glitchless. The new output frequency after a frequency step may have an error of up to 1 ppb more than the frequency error that existed at the previous output frequency. Because the MultiSynth fractional divider has a resolution of nine decimal places, in nearly all cases, the frequency error at the initial frequency is going to be zero.

The maximum clock output frequency in this mode of operation is fVCO/8 where fVCO is the frequency of the device's internal Voltage Controlled Oscillator for the configured frequency plan. If the output frequency is below 5 Mhz, the special considerations in section 2.10 need to be understood. The Si5338 programmer software should be used to set the parameters of the frequency increment/decrement function. When pin control is desired, pins 1 and 2 must be used for the input clock (crystal) so that IN3 and IN4 pins are available to implement the FINC and FDEC functions.

Pin control of frequency requires a positive pulse that is greater than 100 ns followed by at least 100ns of low level. The NVM can be programmed at the factory to set all of the frequency change parameters. Using pin control, the frequency change can occur as fast as 1 MHz. The magnitude of the change must be set using the Si5338 programmer.

Since the Si5338A,B,C,D,E,F devices do not provide pin control of frequency, these devices must use the I^2C interface for this function. Table 14 lists the registers that control the activation of frequency increment and decrement.

Table 14. Output Clock Frequency Control

CLKnFRQSTEPCTRL[1:0] REGISTERS 52,63,74,85[6:5]	Output Frequency
00	Disable all frequency increment/decrement and reset frequency to the initial value.
01	Enable pin control of frequency inc/dec
10	Frequency is incremented
11	Frequency is decremented

Registers 52,63,74,85 control the clock outputs CLK0,1,2,3 respectively. Each single write of 01 to the CLKnFREQSTEPCTRL[1:0] will cause the frequency to be incremented. Likewise a write of 10 will decrement the frequency.

2.10. R Divider Considerations

When the requested output frequency of a channel is below 5 MHz, the Rn (n=0,1,2,3) divider will automatically be set and enabled by the Si5338 Programmer. When the Rn divider is active the step size range of the frequency increment and decrement function will decrease by the Rn divide ratio. The available frequency step size at the input to the Rn divider is 0.1 kHz to 10 MHz. If the Rn divider is set to 16, the frequency step size range at this Rn divider will be 0.1/16 kHz to 10/16 MHz. The Si5338 Programmer will automatically compensate for the frequency step size of the Rn divider. When the Rn divider is set to non-unity, the initial phase of the CLKn output with respect to other CLKn outputs is not guaranteed.

2.11. Spread Spectrum

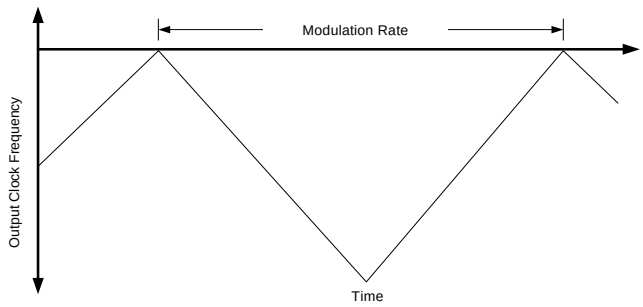


Figure 6. Spread Spectrum Triangle Waveform

To reduce Electro Magnetic Interference (EMI), the Si5338 supports spread spectrum modulation. The output clock frequencies can be modulated to spread energy across a broader range of frequencies, lowering system EMI. The modulation rate is the time required to transition from the maximum spread spectrum frequency to the minimum spread spectrum frequency and then back to the maximum frequency, as shown in Figure 6.

The Si5338 supports 0.5% downspread. The output clocks must be programmed to 100 MHz for this mode of operation. The device supports a modulation rate of 30–33 kHz for compliance with PCI Express applications. Spread spectrum can be enabled or disabled independently for each differential output clock using the CLKn_SSCMODE[1:0] register bits as described in Table 15.

Table 15. Spread Spectrum

CLKn_SSCMODE[1:0] Registers 52,63,74,85	Output Clock
00	No SSC on CLKn
11	Downspread CLKn
Note: All other CLKn_SSCMODE[1:0] settings are reserved.	

2.12. Buffer Mode Operation

The Si5338 can function as a simple 1 or 2 input buffer. In this mode it will also allow translation from one IO format to another as well as dividing the input by up to 1024 using the P and R dividers. The following steps should be followed to configure the Si5338 for buffer mode operation using the Advanced page of the Si5338 Programmer.

1. Disable the PLL
2. Disable all of the MultiSynth dividers
3. Set the CLKIN Frequency to "Off"
4. Set the FDBK Frequency to "Off"
5. Configure the muxes as needed for your application
6. Configure the P and R dividers as needed.

Then go to the Output Drivers Page to select the format of the output drivers.

2.13. Device Reset

The Si5338 supports two reset options. To completely reset the device and clear all contents stored in RAM, use the POR_RESET register bit as shown in Table 16.

Table 16. Power On Reset (POR)

POR_RESET	Description
0	No reset
1	Power on reset (self-clearing)

After any device configuration changes, the device must be soft reset in order for the change to take effect. The soft reset feature is enabled via the SOFT_RESET register bit as shown in Table 17.

Table 17. Soft Reset

SOFT_RESET	Description
0	No reset
1	Calibrates and initiates the device to present configuration.

2.14. Device Interrupt and Alarms

The Si5338 has a maskable interrupt output pin INTR that can be used to monitor the status of the device. Status conditions for system calibration in process, NVM download error, NVM store error, PLL loss of lock (LOL), input clock loss of signal (LOS), and feedback clock LOS can be individually masked to the INTR output pin as shown in Table 18. Each of these status or alarm conditions can also be individually monitored via the read-only registers accessible via the I^2C interface.

The loss of lock algorithm works by continuously monitoring the frequency difference between the input clock frequency and the feedback clock frequency supplied to the device phase frequency detector. When this frequency difference is greater than 1000 ppm, a loss of lock condition is declared. However one must also take into account that the PLL will track a frequency shift/drift of the input clock for up to ~10000 ppm. Hence the input clock frequency may need to be ~11000 ppm in error or more before a LOL condition is declared. The LOS function will assert when the reference clock input signal is removed. When either LOL or LOS occurs, the clock outputs are squelched. When squelched, the output clocks can be programmed to be either a high or a low.

The device always indicates the PLL lock status on the SYS_LOL read-only register bit. The device always indicates the PLL lock status on the INTR pin if the interrupt mask for that bit is not set. To mask an LOL event from appearing on the INTR output pin, set SYS_LOL_MASK to 1. The SYS_LOL register bit is self-clearing once the PLL reasserts lock. A sticky bit is also available for an LOL event (SYS_LOL_STK).The Si5338 monitors the input clock and feedback path for LOS. The LOS algorithm monitors input clock edges and declares an LOS when signal edges are not detected over a 5 µsec observation period. Once a loss of signal event is detected, the device output clocks are squelched. Optional settings to stop the output clock(s) high or low are also available. The device always indicates the loss of signal status on the LOS_CLKIN and LOS_FDBK read-only register bits. The device always indicates the loss of signal status on the INTR pin if the interrupt mask is not set. To mask an LOS event from appearing on the INTR output pin, set LOS_CLKIN_MASK and LOS_FDBK_MASK to 1. The LOS_CLKIN and LOS_FDBK register bits are self-clearing once the clock signal returns and is revalidated. Sticky bits are also available for an LOS alarm (LOS_CLKIN_STK and LOS_FDBK_STK). A loss of signal event will always cause the loss of lock alarm to trigger.

Table 18. Si5338 Status and Alarm Controls

Status/Alarm	Status Register (Read Only, Self-Clearing)	Sticky Bit Register	Mask Register
System Calibration in Process	SYS_CAL	SYS_CAL_STK	SYS_CAL_MASK
NVM Download Error	NVM_DLD_ERR	NVMERR_STK	NVMERR_MASK
NVM Store Error	NVM_STORE_ERR	NVMSTORE_STK	NVMERR_MASK
PLL Loss of Lock	SYS_LOL	SYS_LOL_STK	SYS_LOL_MASK
CLKIN± Loss of Signal	LOS_CLKIN	LOS_CLKIN_STK	LOS_CLKIN_MASK
FDBK± Loss of Signal	LOS_FDBK	LOS_FDBK_STK	LOS_FDBK_MASK

2.15. Self-Calibration

The device performs an internal self-calibration before operation to optimize loop parameters and jitter performance. While the self-calibration is being performed, the device VCO is being internally controlled by the self-calibration state machine and the LOL alarm is masked. The output clocks appear after the device finishes self calibration.

The following events will trigger a self-calibration by default.

- Power on reset (POR_RESET)
- Soft reset (SOFT_RESET)
- Loss of signal (LOS)
- Loss of lock (LOL)

2.16. Device Programming

Figure 7 shows the sequence of steps that must be used after a power-on reset to ensure proper device operation.

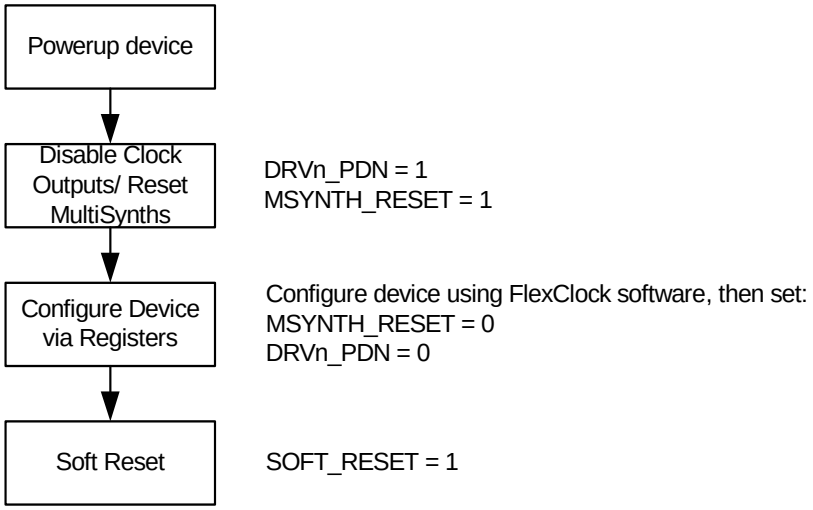


Figure 7. Si5338 Programming Sequence

2.17. Register Descriptions

See the Si5338 Register Map file for a full description of the device registers.

2.18. I²C Interface

The Si5338 control interface is a 2-wire bus for bidirectional communication. The bus consists of a bidirectional serial data line (SDA) and a serial clock input (SCL). The device operates as a slave device on the 2-wire bus and is compatible with I²C specifications. Both lines must be connected to the positive supply via an external pull-up. Standard-Mode (100 kbps) and Fast-Mode (400 kbps) and Fast Mode+ (1000 kbps) operation and 7-bit addressing are supported as specified in the I²C-Bus Specification standard. To accommodate multiple Si5338 devices on the same I²C bus, the Si5338A/B/C has pin 4 as I2C_LSB.

The complete bus address for the device is as follows:

0111 000[I2C_LSB].

See Figure 1 and Figure 2 for the command format for both read and write access. Data is always sent MSB first. Table 9 includes the AC and DC electrical parameters for the SCL and SDA I/Os, respectively. The timing specifications and timing diagram for the I²C bus can be found in the I²C-Bus Specification standard. Go to the following URL:

http://www.nxp.com/acrobat_download/usermanuals/UM10204_3.pdf. SDA timeout support is supported for compatibility with SMBus interfaces. The I²C interface is 3.3 V tolerant.

The I²C bus can be operated at a bus voltage of 1.71 to 3.63 V and should have a pullup resistor of no larger than 1 kΩ. When the I²C bus is operated at a voltage below 2.25 V, the input threshold of pin 19 must be changed by writing register 27[7] = 1.

2.19. Field/Factory Programming Options

The Si5338 any-rate clock generator supports a customer-accessible one-time programmable NVM for field programming. This optional feature allows users to specify the startup configuration of the device. Following device programming and a subsequent POR, the device will come up in this new default configuration. This feature is available through the customer programming kit (Si5338-PROG-EVB) and the Si5338 configuration software. Once the default profile is written, it cannot be changed. Note that the device supply voltage must be set to 3.6 V during a NVM write.

2.19.1. Si5338 Programmable Default Configuration

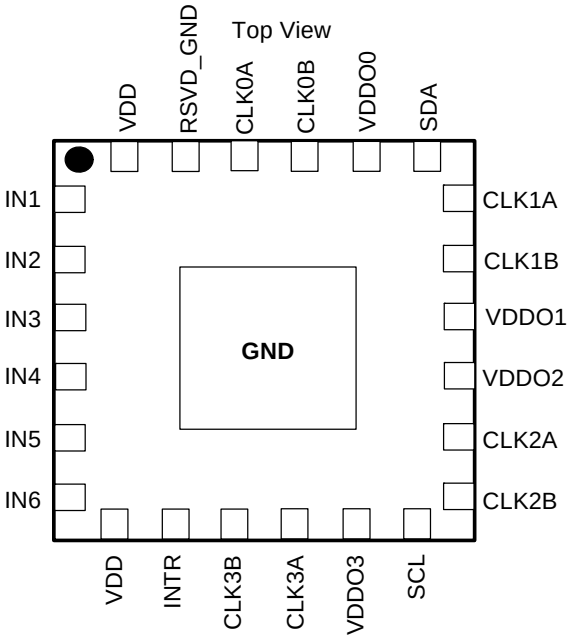
The Si5338 configuration software can be used to order factory-programmed Si5338 clock generators with user-specified startup configurations. The output of the Si5338 software is a device configuration file. This file can be sent to Silicon Labs and a unique Si5338 part number assigned. Subsequent production orders for a custom I^2C-programmable Si5338 clock generator are fulfilled by factory programming. Certain restrictions apply. Contact your local Silicon Labs sales representative for more information.

2.19.2. Si5334 Pin-Controlled Clock Generator

In applications in which an I^2C interface is not available, Silicon Labs offers custom pin-controlled clock generators. The Si5338 programming kit (Si5338-PROG-EVB) is used to field-program pin-controlled clock generators for initial device testing and qualification. Five Si5338 samples are provided with each programming kit for this purpose. After the device configuration is finalized, an Si5338 can be field-programmed as an Si5334 pin-controlled clock generator.

The output of the Si5338 software is a device configuration file. This file can be sent to Silicon Labs and a unique Si5334 part number assigned. Subsequent production orders for custom Si5334 pin-controlled clock generators are fulfilled by factory programming. Certain restrictions apply. Contact your local Silicon Labs sales representative for more information.

3. Pin Descriptions—Si5338



Note: Center pad must be tied to GND for normal operation.

Table 19. Si5338 Pin Descriptions

Pin #	Pin Name	I/O	Signal Type	Description
1	IN1	I	Multi	**GND** If a single ended clock is input on pin 3, then pins 1 and 2 are unused and should be tied to GND.
2	IN2	I	Multi	**CLKIN** If a crystal is used connect it across pins 1 and 2. If a differential clock is input, AC couple it to these pins. When used as a differential input, a 100 ohm resistor should be placed across these pins and located very close to the device.

Table 19. Si5338 Pin Descriptions (Continued)

Pin #	Pin Name	I/O	Signal Type	Description
3	IN3	I	Multi	**CLKIN** High impedance input for single ended signals such as CMOS, SSTL or HSTL. The input should be dc-coupled. **PINC** This pin function is active for devices Si5338D/E/F. A positive pulse of greater than 100ns width (followed by >100 ns low) will increase the input to output device latency by a programmed amount. The effect of this pin can be preprogrammed at the factory and/or the I^2C interface can also be used to set the function of this pin. **FINC** This pin function is active for devices Si5338G/H/J. A positive pulse of greater than 100 ns width (followed by >100ns low) will increase the output frequency of the clock output by a programmed amount. The function of this pin can be preprogrammed at the factory and/or the I^2C interface can also be used.
4	IN4	I	Multi	**I2C_LSB** This pin is the LSB of the Si5338 I^2C address. **PDEC** This pin function is active for devices Si5338D/E/F. A positive pulse of greater than 100 ns width (followed by >100ns low) will decrease the input to output device latency by a programmed amount. The function of this pin can be preprogrammed at the factory and/or the I^2C interface can also be used to set the function of this pin. **FDEC** This pin function is active for devices Si5338G/H/J. A positive pulse of greater than 100ns width (followed by >100ns low) will decrease the output frequency of the clock output by a programmed amount. The effect of this pin can be preprogrammed at the factory and/or the I^2C interface can also be used.
5	IN5	I	Multi	**GND** If a zero delay buffer is not implemented, this pin should be connected to GND. **FDBK** In zero delay buffer mode, one side of a differential input should be supplied to this pin. The other side of the differential input should be supplied to IN6. This pin functions as the feedback clock input for the PLL phase frequency detector.

Table 19. Si5338 Pin Descriptions (Continued)

Pin #	Pin Name	I/O	Signal Type	Description
6	IN6	I	Multi	**GND** In clock generator mode, this pin functions as a GND pin. It must be tied low. **FDBKB** In zero delay buffer mode, one side of a differential input should be supplied to this pin. The other side of the differential input should be supplied to IN5. This pin functions as the feedback clock input for the PLL phase frequency detector.
7	VDD	VDD	Supply	**Core Supply Voltage** The device operates from a 1.8, 2.5, or 3.3 V supply. A 0.1 µF bypass capacitor should be located very close to this pin.
8	INTR	O	Open Drain	**Interrupt** This pin functions as a maskable interrupt output. 0 = No interrupt. 1 = Interrupt present. This pin requires an external ≤1 kΩ pull-up resistor.
9	CLK3B	O	Multi	**Output Clock B for Channel 3** May be a single-ended output or half of a differential output with CLK3A being the other differential half.
10	CLK3A	O	Multi	**Output Clock A for Channel 3** May be a single-ended output or half of a differential output with CLK3B being the other differential half.
11	VDDO3	VDD	Supply	**Output Clock Supply Voltage** Supply voltage for CLK3A,B. If CLK3 is not used, this pin must be tied to pin 7 and/or pin 24.
12	SCL	I	LVCMOS	**I^2C Serial Clock Input**
13	CLK2B	O	Multi	**Output Clock B for Channel 2** May be a single-ended output or half of a differential output with CLK2A being the other differential half.
14	CLK2A	O	Multi	**Output Clock A for Channel 2** May be a single-ended output or half of a differential output with CLK2B being the other differential half.
15	VDDO2	VDD	Supply	**Output Clock Supply Voltage** Supply voltage for CLK2A,B. If CLK2 is not used, this pin must be tied to pin 7 and/or pin 24.
16	VDDO1	VDD	Supply	**Output Clock Supply Voltage** Supply voltage for CLK1A,B. If CLK1 is not used, this pin must be tied to pin 7 and/or pin 24.
17	CLK1B	O	Multi	**Output Clock B for Channel 1** May be a single-ended output or half of a differential output with CLK1A being the other differential half. If unused, this pin must be tied to VDD pin 24.

Table 19. Si5338 Pin Descriptions (Continued)

Pin #	Pin Name	I/O	Signal Type	Description
18	CLK1A	O	Multi	**Output Clock A for Channel 1** May be a single-ended output or half of a differential output with CLK1B being the other differential half.
19	SDA	I/O	LVCMOS	**I^2C Serial Data**
20	VDDO0	VDD	Supply	**Output Clock Supply Voltage** Supply voltage for CLK0A,B. If CLK2 is not used, this pin must be tied to pin 7 and/or pin 24.
21	CLK0B	O	Multi	**Output Clock B for Channel 0** May be a single-ended output or half of a differential output with CLK0A being the other differential half. If unused, this pin must be tied to VDD pin 24.
22	CLK0A	O	Multi	**Output Clock A for Channel 0** May be a single-ended output or half of a differential output with CLK0B being the other differential half.
23	RSVD_GND	GND	GND	**Ground.** Must be connected to system ground. Minimize the ground path impedance for optimal performance of this device.
24	VDD	VDD	Supply	**Core Supply Voltage.** The device operates from a 1.8, 2.5, or 3.3 V supply. A 0.1 µF bypass capacitor should be located very close to this pin.
GND PAD	GND	GND	GND	**Ground Pad.** This is the large pad in the center of the package. Nine or more vias should be used to connect this pad to a ground plane. Device specifications cannot be guaranteed unless the ground pad is properly connected to a ground plane on the PCB.

4. Device Pinout by Part Number

Si5338A/D/G/K have a maximum frequency limit of 700 MHz. Si5338B/E/H/L have a maximum frequency of 350 MHz. Si5338C/F/J/M have a maximum frequency of 200 MHz.

All Si5338 versions can have their reference clock come from a crystal oscillator or from a an onboard differential input clock. In addition, all Si5338 versions can be used as a zero delay buffer by having CLK3A/B feed back to pins 5 and 6.

TheSi5338A/B/C can be ordered to use a differential or a single-ended input clock and will have the I2C_LSB bit on pin 4.

The Si5338D/E/F has the phase increment and decrement function available as pins. The Si5338G/H/J has the frequency increment/decrement function available as pins. The Si5338K/L/M has the output enable (OEB) on pin 3 and the I2C_LSB on pin 4.

Pin #	Part Number/Pin Function				
	Common Pin Name	**Si5338A/B/C**	**Si5338D/E/F**	**Si5338G/H/J**	**Si5338K/L/M**
1	IN1	CLKIN	CLKIN	CLKIN	CLKIN
2	IN2	CLKINB	CLKINB	CLKINB	CLKINB
3	IN3	CLKIN	PINC	FINC	OEB
4	IN4	I2C_LSB	PDEC	FDEC	I2C_LSB
5	IN5	GND/FDBK	GND/FDBK	GND/FDBK	GND/FDBK
6	IN6	GND/FDBKB	GND/FDBKB	GND/FDBKB	GND/FDBKB
7	VDD				
8	INTR				
9	CLK3B				
10	CLK3A				
11	VDDO3				
12	SCL				
13	CLK2B				
14	CLK2A				
15	VDDO2				
16	VDDO1				
17	CLK1B				
18	CLK1A				
19	SDA				
20	VDDO0				
21	CLK0B				
22	CLK0A				
23	GND				
24	VDD				

5. Package Outline: 24-Lead QFN

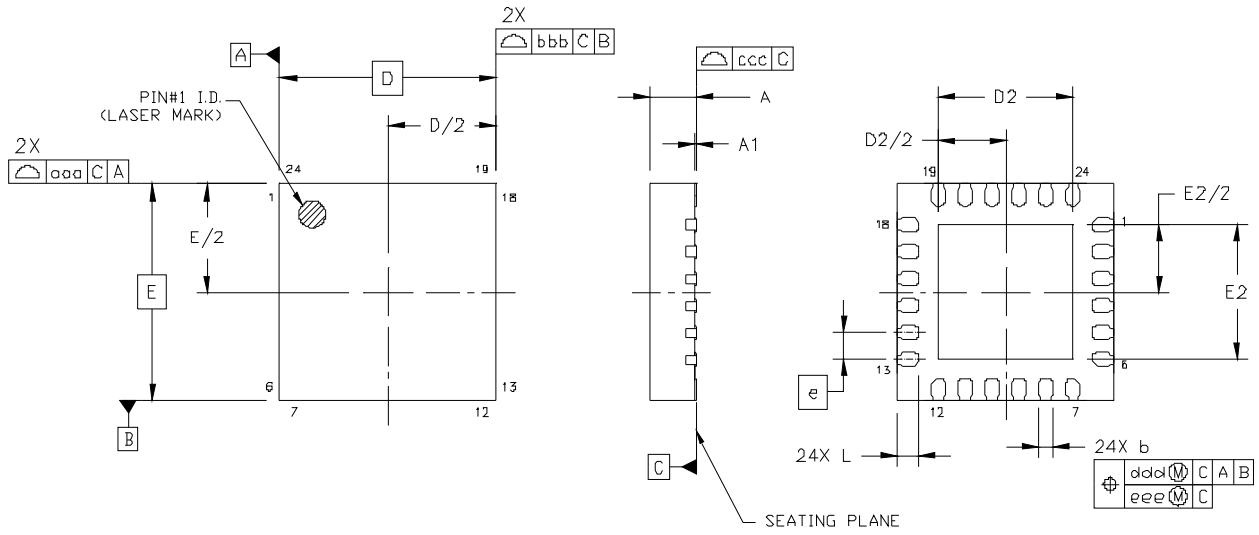


Figure 8. 24-Lead Quad Flat No-lead (QFN)

Table 20. Package Dimensions

Dimension	Min	Nom	Max
A	0.80	0.85	0.90
A1	0.00	0.02	0.05
b	0.18	0.25	0.30
D		4.00 BSC.	
D2	2.35	2.50	2.65
e		0.50 BSC.	
E		4.00 BSC.	
E2	2.35	2.50	2.65
L	0.30	0.40	0.50
aaa		0.10	
bbb		0.10	
ccc		0.08	
ddd		0.10	
eee		0.05	

Notes:

1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. Dimensioning and Tolerancing per ANSI Y14.5M-1994.
3. This drawing conforms to the JEDEC Outline MO-220, variation VGGD-8.
4. Recommended card reflow profile is per the JEDEC/IPC J-STD-020C specification for Small Body Components.

6. Recommended PCB Layout

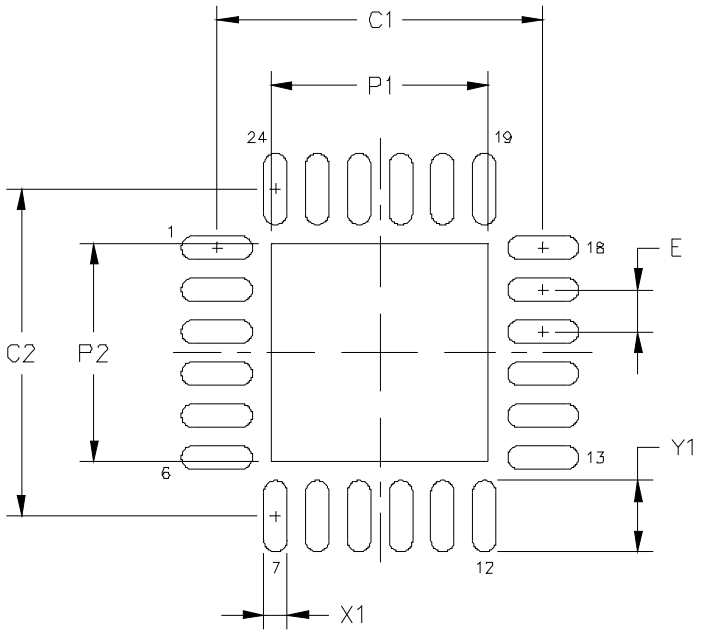


Table 21. PCB Land Pattern

Dimension	Min	Nom	Max
P1	2.50	2.55	2.60
P2	2.50	2.55	2.60
X1	0.20	0.25	0.30
Y1	0.75	0.80	0.85
C1	3.90		
C2	3.90		
E	0.50		

Notes:

General

1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. Dimensioning and Tolerancing per ANSI Y14.5M-1994 specification.
3. This Land Pattern Design is based on the IPC-7351 guidelines.

Solder Mask Design

4. All metal pads are to be non-solder mask defined (NSMD). Clearance between the solder mask and the metal pad is to be 60 µm minimum, all the way around the pad.

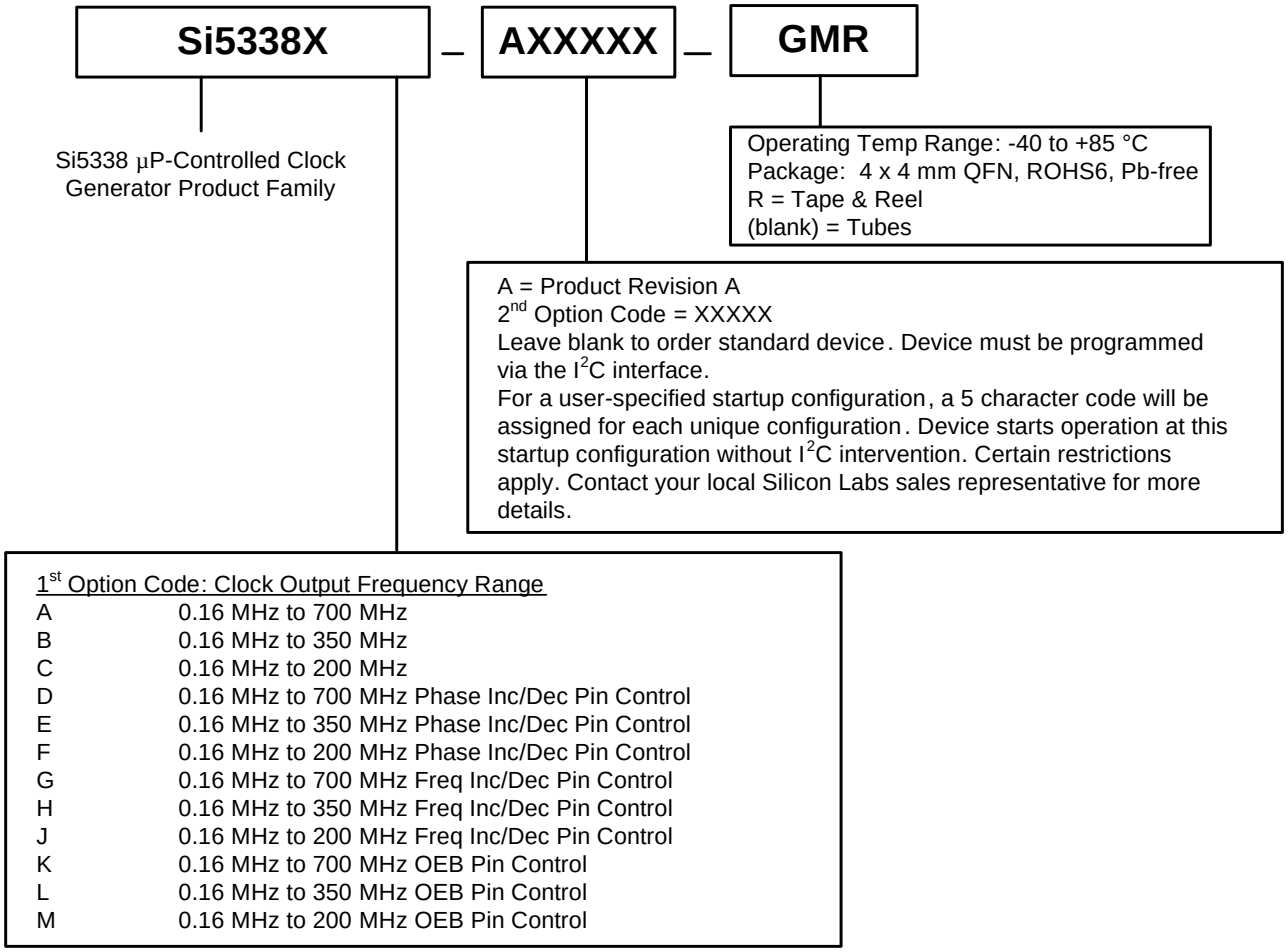
Stencil Design

5. A stainless steel, laser-cut and electro-polished stencil with trapezoidal walls should be used to assure good solder paste release.
6. The stencil thickness should be 0.125mm (5 mils).
7. The ratio of stencil aperture to land pad size should be 1:1 for all perimeter pins.
8. A 2x2 array of 1.0 mm square openings on 1.25mm pitch should be used for the center ground pad.

Card Assembly

9. A No-Clean, Type-3 solder paste is recommended.
10. The recommended card reflow profile is per the JEDEC/IPC J-STD-020C specification for Small Body Components.

7. Ordering Information


Si5338X
AXXXXX
GMR
Si5338 µP-Controlled Clock Generator Product Family
Operating Temp Range: -40 to +85 °C
Package: 4 x 4 mm QFN, ROHS6, Pb-free
R = Tape & Reel
(blank) = Tubes
A = Product Revision A
2nd Option Code = XXXXX
Leave blank to order standard device. Device must be programmed via the I2C interface.
For a user-specified startup configuration, a 5 character code will be assigned for each unique configuration. Device starts operation at this startup configuration without I2C intervention. Certain restrictions apply. Contact your local Silicon Labs sales representative for more details.
1st Option Code: Clock Output Frequency Range
A 0.16 MHz to 700 MHz
B 0.16 MHz to 350 MHz
C 0.16 MHz to 200 MHz
D 0.16 MHz to 700 MHz Phase Inc/Dec Pin Control
E 0.16 MHz to 350 MHz Phase Inc/Dec Pin Control
F 0.16 MHz to 200 MHz Phase Inc/Dec Pin Control
G 0.16 MHz to 700 MHz Freq Inc/Dec Pin Control
H 0.16 MHz to 350 MHz Freq Inc/Dec Pin Control
J 0.16 MHz to 200 MHz Freq Inc/Dec Pin Control
K 0.16 MHz to 700 MHz OEB Pin Control
L 0.16 MHz to 350 MHz OEB Pin Control
M 0.16 MHz to 200 MHz OEB Pin Control

DOCUMENT CHANGE LIST

Revision 0.1 to 0.2

- Updated block diagram to show Rn output divider and PLL bypass mode
- Updated pin description to include FDBK±
- Updated Table 2. DC Characteristics
- Updated Table 8. Jitter Specifications
- Added Figure 3. Supply Current vs. Output Frequency
- Updated package outline specification
- Clarified input clock configuration register settings
- Updated DRV_INVERTn[1:0] settings
- Added PLL bypass mode
- Added LOS_FDBK description
- Added additional detail to phase increment/ decrement and frequency increment/decrement descriptions
- Clarified output driver powerdown options
- Clarified entry to self-calibration mode
- Updated ordering guide

Revision 0.2 to 0.3

- Changed minimum output clock frequency from 5 MHz to 1 MHz.
- Updated slew rates.
- Updated " Features" on page 1.
- Updated Table 3, “Input and Output Clock Characteristics,” on page 6.
- Deleted Table 12, “Output Driver Slew Rate Control,” on page 17.

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